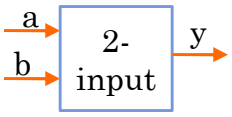
Introduction to FPGA Architecture

Digital Logic Design (Basic Techniques)



Black Box

$$y = a.b$$

Functional

Schematic

a	b	y
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table (AND)

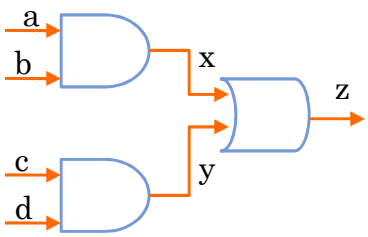
a	b	y
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table (OR)

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table (XOR)

DIGITAL LOGIC DESIGN



a	b	x
0	0	0
0	1	0
1	0	0
1	1	1

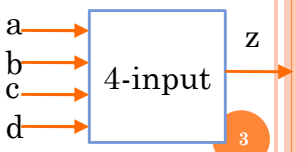
Gate Level Implementation is specified

c	d	y
0	0	0
0	1	0
1	0	0
1	1	1

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

a	b	c	d	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
…	…	…	…	…
1	1	1	0	1
1	1	1	1	1

Gate Level Implementation not specified



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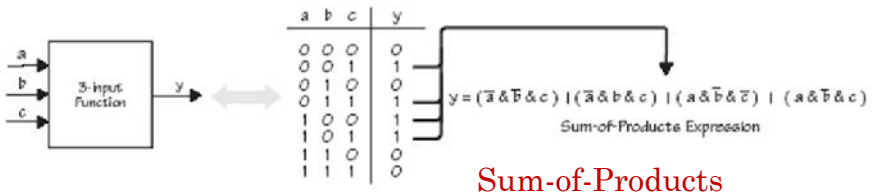
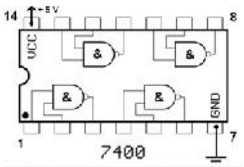
DIGITAL LOGIC DESIGN



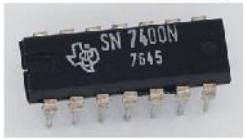
Sum-of-Products Expression



Connect Standard Logic Chips Very Simple Glue Logic

FIXED Logic

- Fixed Architecture
- Fixed Delay



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PROGRAMMABLE LOGIC (PLDS)

A PLD consists of an array of AND gates and an array of OR gates

Each input feeds both a non-inverting buffer and an inverting
buffer to produce the true and inverted forms of each variable.
(i.e. the input lines to the AND-gate array)

The AND outputs are called the product lines

Each product line is connected to one of the inputs of each OR

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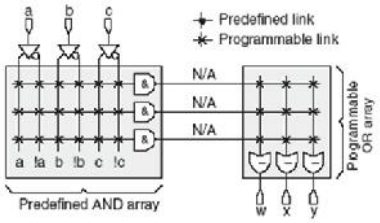
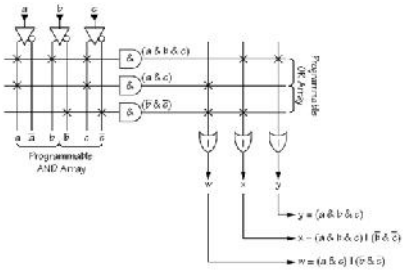
PROGRAMMABLE LOGIC (PLDS)



Planes of ANDs and ORs



Programmed State

- **Prefabricated**
- **Programmble Links**
- **Reconfigurable**

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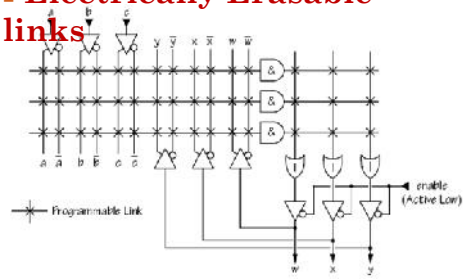
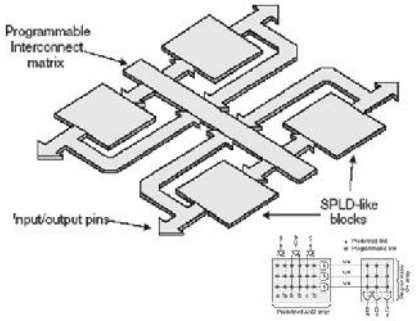
Complex PLDs

- **Programmable PLD Blocks**
- **Programmable Interconnects**
- **Electrically Erasable links**



Feedback Outputs



CPLD Architecture

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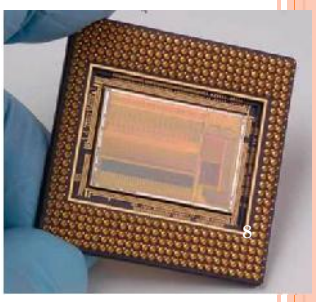
ASIC

Application Specific Integrated Circuits

- Customized for a particular use
- e.g. digital voice recorder
- May include from 5k to 100 million of gates
- Often include entire microprocessor, memory blocks and other large building blocks.



COMPARISON

PLDs		ASIC
Limited Complexity	The GAP	Large Complex Functions
Thousands of Gates		Customized of Extreme speed, low power
Cheap		Expensive (in small quantities) > $ 1 million mask set
Easy to Design		Hard to Design Long design cycle
Reprogrammable		NOT Reprogrammable. HIGH RISK

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COMPARISON

PLDs		ASIC
Limited Complexity	 **FPGA**	Large Complex Functions
Thousands of Gates	Large Complex Functions	Customized of Extreme speed, low power
Cheap	Inexpensive	Expensive (in small quantities) > $ 1 million mask set
Easy to Design	Easy to Design	Hard to Design Long design cycle
Reprogrammable	Reprogrammable	NOT Reprogrammable. HIGH RISK

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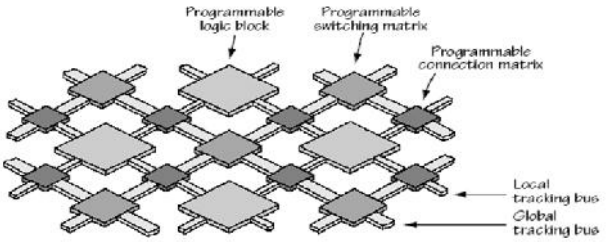
What is FPGA?

- An FPGA is made up of an array of programmable logic blocks.
- These logic blocks are connected by reconfigurable sets of wires.
- These wires allow for signals to be routed according to the definition of the circuit.
- The circuits are defined by a user in a programming language, specifically intended to describe hardware.



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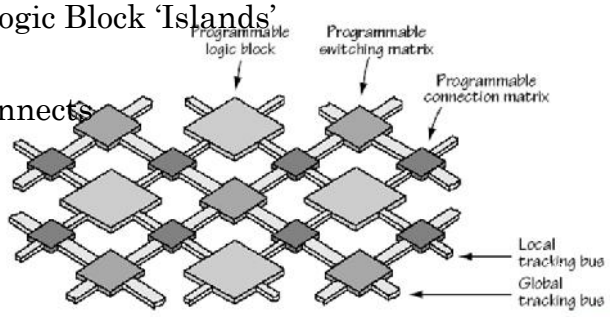
Field Programmable Gate Arrays

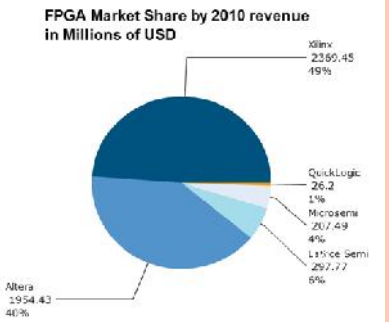
- Field Programmable Gate Array
  - New Architecture
  - 'Simple' Programmable Logic Blocks
  - Massive Fabric of Programmable Interconnects

Large Number of Logic Block 'Islands'
1,000 … 100,000+
in a 'Sea' of Interconnects

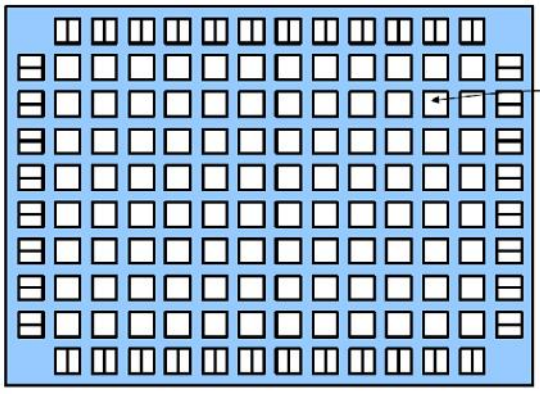


Major Vendors

- Xilinx & Altera are two major vendors of FPGAs.
- They hold almost 89% of the FPGA market.
- Both companies offer a good range of FPGAs in terms of cost and performance.
- For Xilinx, Spartan series covers the low-to-mid-end market while the Virtex series covers the high-end.



Inside FPGA

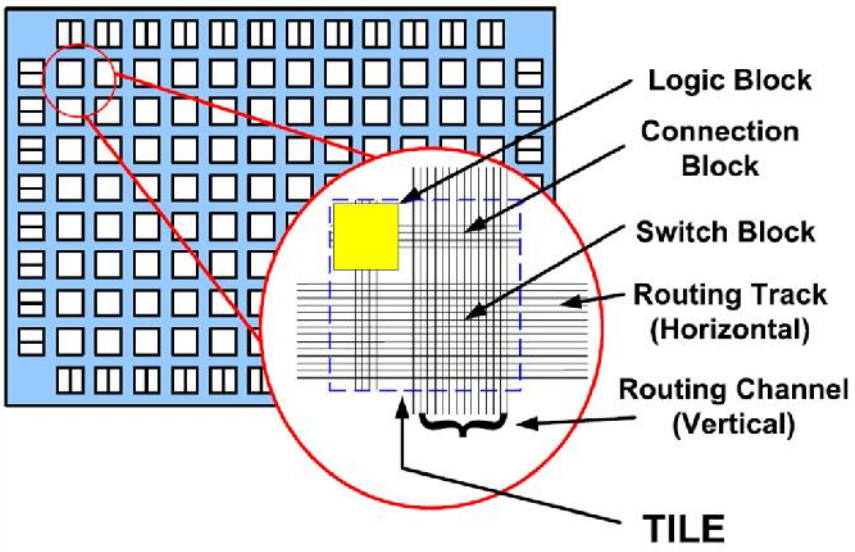


Logic Blocks
- used to implement logic
- lookup tables, LUTs and flip-flops

Altera: LABs

Xilinx: CLBs

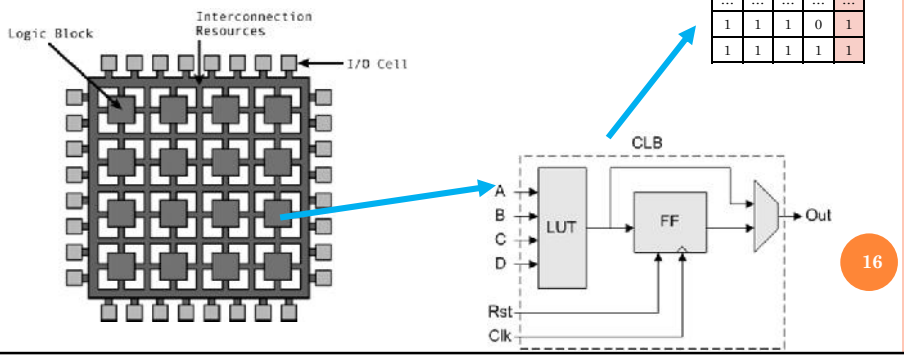
INSIDE FPGA?



CLB ARCHITECTURE

- Logic Functions implemented in Lookup Table LUTs
- Multiplexers (select 1 of N inputs)
- Flip-Flops. Registers. Clocked Storage elements.

a	b	c	d	z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
…	…	…	…	…
1	1	1	0	1
1	1	1	1	1



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FPGAs

- In Past, FPGAs were marketed for primarily two uses
  - For prototyping ASICs.
  - To achieve time-to-market, knowing that an ASIC implementation will replace ASAP.
- FPGAs can be programmed on your desk top in minutes while ASICs require weeks to fabricate a new design.
- With advancements in technology
  - FPGAs design capacity increased enormously.
  - FPGA speeds increased
  - Power consumption decreased
  - And prices decreased

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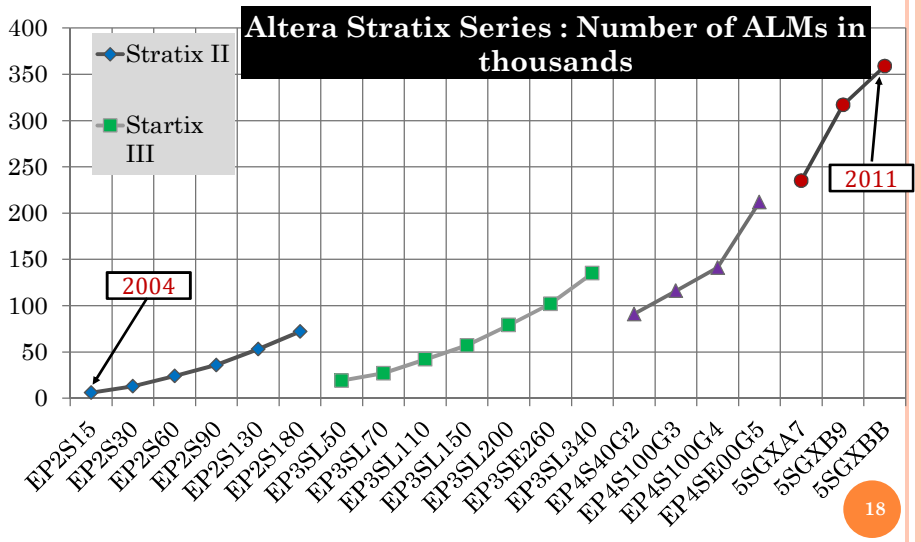
FPGAs Logic Density (Altera's Stratix Series)



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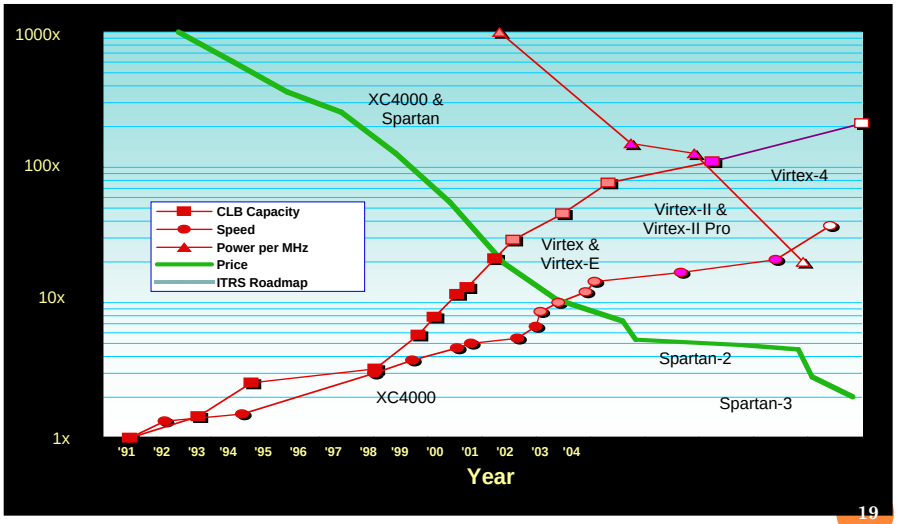
CLB Price, density (Xilinx FPGAs)



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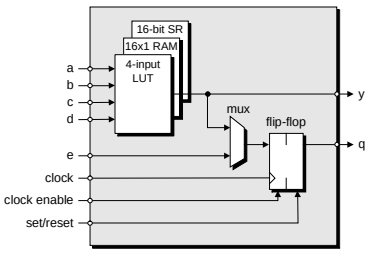
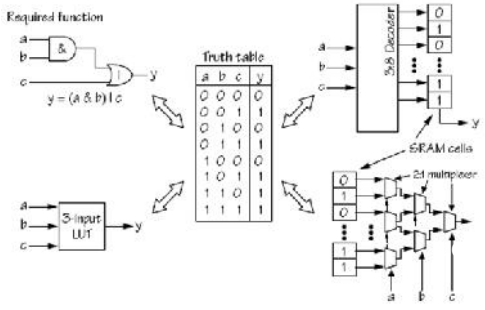
Logic Block cost ~ 1$ in 1990 ; $0.002 in 2005

Lookup Tables LUTs

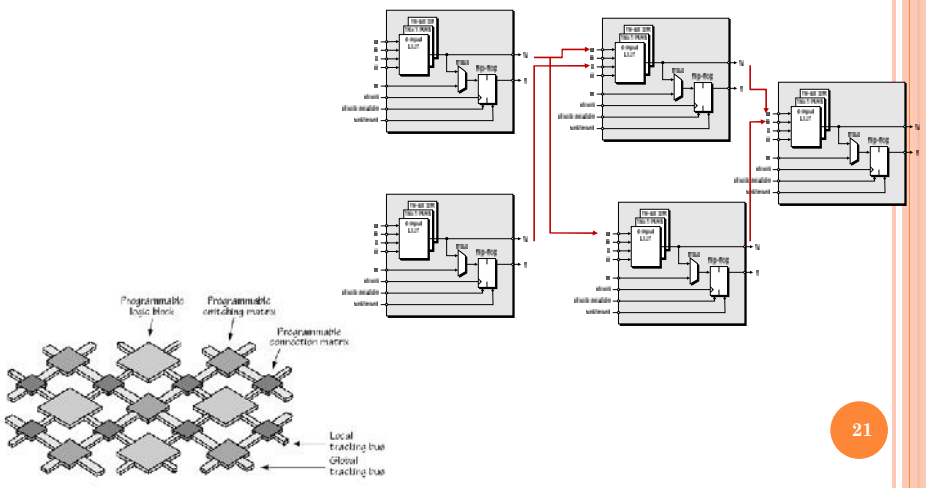
- LUT contains Memory Cells to implement small logic functions
- Each cell holds '0' or '1' .
- Programmed with outputs of Truth Table
- Inputs select content of one of the cells as output





Logic Blocks

Larger Logic Functions built up by connecting many Logic Blocks together



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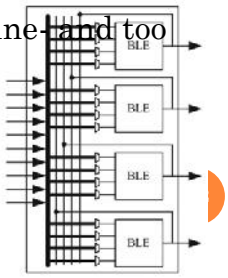
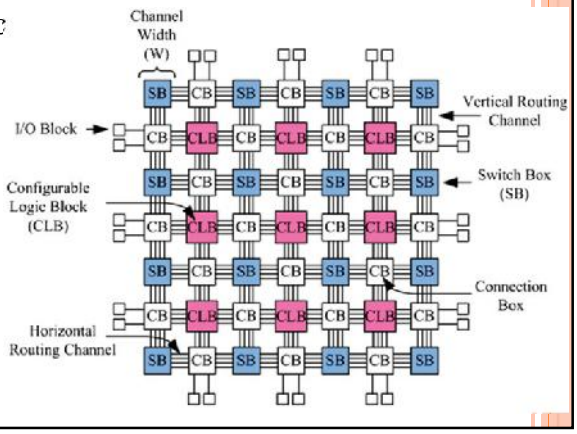
Coarse- Vs Fine-grained CLBs

- A CLB can be either a *transistor* or a complete *processor*. [2 extremes]
- Very fine-grained CLB requires a large amount of programmable interconnects
  - Low performance, higher power consumption
- Coarse-grained CLB can not be used to implement small functions.
  - Wastage of resources.
- LUT-based CLB provides trade-off b/w too fine- and too coarse-architecture.
- A CLB can comprise of
  - A single Basic Logic Element (BLE)
  - A cluster of locally connected BLEs.

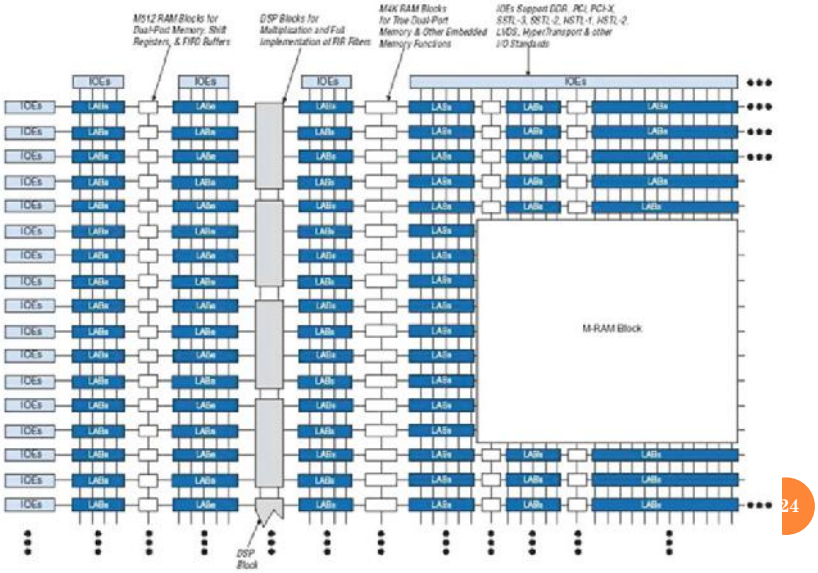


Routing Architecture

- The flexibility of an FPGA mainly dependent on the routing network.
- Routing network occupies 80-90% of Area.
- Switch Box interconnects Horizontal and Vertical Channels.
- Connection Box connec



Altera's Stratix II



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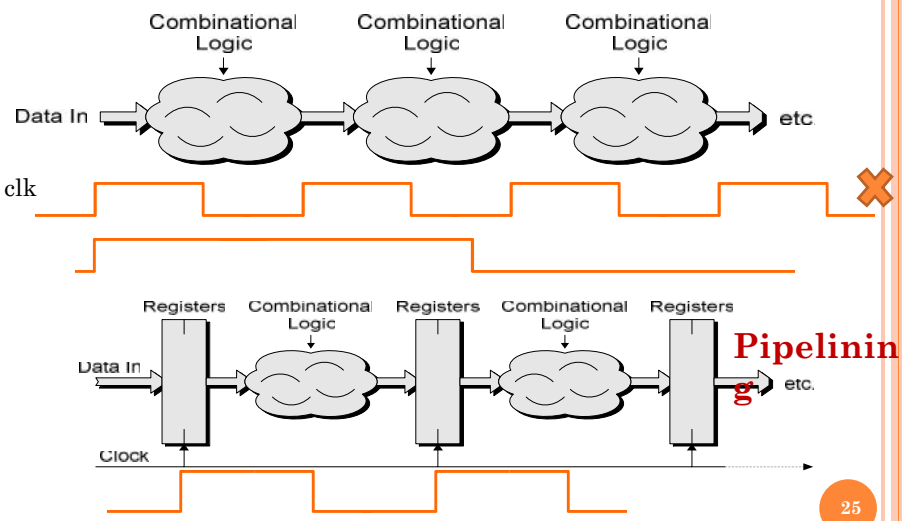
FPGA Design Synchronous Logic



Pipelining

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Register Transfer Logic RTL

Design Flow

Circuit described in HDL (Verilog/Vhdl)

Transforms HDL to set of Boolean gates & FFs OR (DAG)

Implements DAG using Library cells

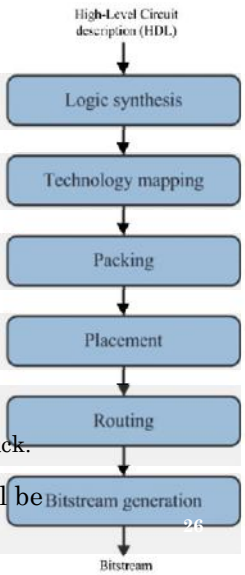
Forms Clusters of Logic Blocks to implement in a CLB

Assigns Logic CLBs to Physical CLBs

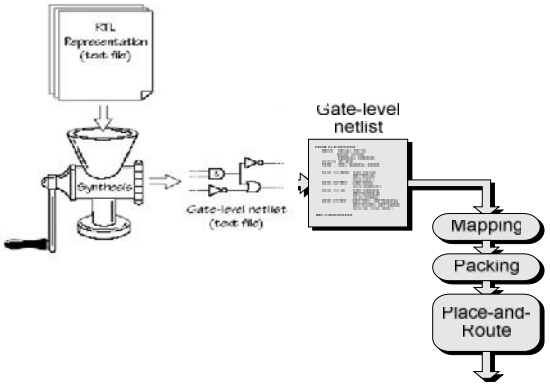
Routing: Assigns nets to routing resources

Timing Analysis: Analyze speed of circuit and determines the slack.

Bitstream contains information as which SRAM bit will be '0' or '1'.



Design Flow



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Conclusion

Till now, We have discussed

- A pathway from digital logic designing to FPGAs
- FPGA architecture
- Basic Logic Block Architecture
- Pipelining
- Software Design Flow

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SPARTAN-3E FAMILY

• Sparatan-3E family by Xilinx, targets cost-sensitive applications.
• The five family members provide density ranging from 100K to 1.6 million gates.
• Spartan-3E architecture consists of 5 fundamental elements.

1. Configurable Logic Block (CLB).
2. Input/Output Blocks (IOBs)
3. Block RAM
4. Multiplier Block
5. Digital Clock Manager (DCMs)

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits[1]	Block RAM bits[1]	Dedicated Multipliers	DCMs	Maximum User I/O
			Rows	Columns	Total CLBs	Total Slices					
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376

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- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

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SPARTAN-3E ARCHITECTURE

These elements are organized in the following manner.

- A ring of IOBs surrounds a regular array of CLBs.
- Each device has two columns of block RAM except for the XC3S100E, which has one column.
- Each RAM column consists of several 18-Kbit RAM blocks.
- Each block RAM is associated with a dedicated multiplier.
- The DCMs are positioned in the center with two at the top and two at the bottom of the device.
- The XC3S100E has only one DCM at the top and bottom
- The XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

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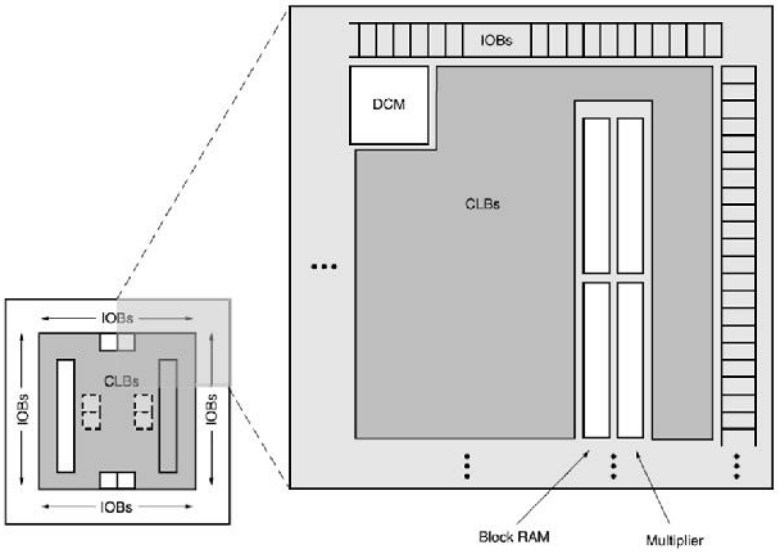
SPARTAN-3E FAMILY ARCHITECTURE



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CLB Architecture

Each CLB consists of 4 Slices, while each slice contains:

i. 2 4-input Look Up Tables (LUTs).
ii. 2 storage elements.
iii. 2 multiplexers.
iv. Carry and Arithmetic logic

Two of these four slices, within a CLB, also contains memory elements:

i. 2 16x1 RAM Block
ii. 2 16-bit shift registers.

Thus, half of the slices supports both memory and logic functions, while the other half supports only logic function