SIR SYED UNIVERSITY OF ENGINEERING & TECHNOLOGY
ELECTRONIC ENGINEERING DEPARTMENT

COURSE INFORMATION SHEET
(For Theory + Lab Based Course)

Session:	Spring-2022
Course Title:	Embedded System Design and Application
Course Code:	EE – 423
Credit Hours:	3+1
Semester:	7th
Pre-Requisites:	EE-320 Microprocessor & Microcontroller systems
Instructor Name:	*Shiraz Afzal*
Email and Contact Information:	*safzal@ssuet.edu.pk*
WhatsApp Group	Embedded System
Office Hours:	8:30am to 5:00pm
Mode of Teaching:	Synchronous/Asynchronous/ Hybrid/Blended

COURSE OBJECTIVE:

The objective of this course is to enable the students to understand embedded-system programming and apply that knowledge to design and develop embedded solutions. To develop the understanding of embedded system architecture and peripheral interfacing techniques including PIC Microcontroller, Arduino and FPGA. To develop familiarity with tools, languages like Assembly, HDL and C Language used to develop in an embedded environment.

COURSE OUTLINE:

Trends and challenges in embedded system design, Advanced Microcontrollers including PIC architecture and programming. Design and development of hardware and software for standalone embedded systems using FPGA Comparative analysis of various embedded systems for a given engineering problem.

COURSE LEARNING OUTCOMES (CLOs) and its mapping with Program Learning Outcomes (PLOs):

CLO No.	Course Learning Outcomes (CLOs)	PLOs	Bloom's Taxonomy
1	**Comprehend** the basic knowledge of embedded system and its architecture included PIC Microcontroller and FPGA.	PLO_1 (Engineering Knowledge)	C2 (Understand)
2	**Demonstrate** programming interfacing of PIC Microcontroller and FPGA with different type of peripherals.	PLO_2 (Problem Analysis)	C3 (Apply)
3	**Design** an embedded system based solution for the engineering problem.	PLO_3 (Design/ Development of solutions)	C6 (Create)
4	**Follow** the design methodology to interface peripheral for different application of embedded system.	PLO_3 (Design/Development of Solutions)	P3 (Guided Response)
5	**Present** solution to serve an engineering problem.	PLO_10 (Communication)	A2 (Responding to Phenomena)

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COMPLEX ENGINEERING PROBLEM/ACTIVITY:

Complex Engineering Problem Details	**Included: Yes** Nature and details of Complex Engineering Problem (CEP): It will be given in Assignment # 03. CEP will be based on CLO-3 "Students have to develop learning about "**Design** an embedded system based solution for the engineering problem". To solve the problem student have to use in-depth knowledge related to the following concepts: Finite state machine, Moore machine FSM, mealy machine FSM, state diagram and VHDL language **Attributes could be: WP1, WP3, WK5, WK8** WP1: Depth of knowledge required WP3: Depth of analysis required WK5: Engineering Design WA3: Design/Development of Solutions Assessment in: Assignment # 03
Complex Engineering Activity Details	**Included: Yes** Activity: Project Assigned to 2-3 students in a group Provide the complete details of the Complex Engineering Activity along with the Attributes.

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RELATIONSHIP BETWEEN ASSESSMENT TOOLS AND CLOs:

Assessment Tools	CLO-1(24)	CLO-2(32)	CLO-3(24)	CLO-4(15)	CLO-5(05)
Quizzes	8.33% (2)	3.125% (1)	8.33% (2)		
Assignments	8.33% (2)	3.125% (1)	8.33% (2)		
Midterm Exam	41.66% (10)	31.25% (10)	-		
Final Exam	41.66% (10)	62.5% (20)	83.3% (20)		
Lab Assessment	-	-	-	100% (15)	100% (5)

GRADING POLICY:

Assessment Tools	Percentage
Quizzes	5%
Assignments	5%
Midterm Exam	20%
Final Exam	50%
Lab Assessment	20%
TOTAL	**100%**

Recommended Book:

- Muhammad Ali Mazidi, *PIC Microcontroller & Embedded System*, Pearson international edition.
- Wayne Wolf, *FPGA-Based System Design*, 1st Edition, 2004, Pearson Prentice Hall
- Juline Bayle, *C Programming for Arduino.*

Reference Books:

- Stephen Brown, *Fundamental of digital Logic with VHDL design,* 2nd Edition 2005, Mc Graw Hill

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COURSE BREAKDOWN WITH LAB SYNCHRONIZATION:

- **Both sides same Colours:** Lab is synchronized with the topic
- **Red Color:** Lab is not synchronized (*conducted before theory*)
- **No Color:** Lab is to introduce new hardware or software skill / Open Ended Lab / Lab is relevant to a topic taught in pre-requisite and required for upcoming labs

Week No.	Topics	Laboratory Synchronization
1	PIC Microcontrollers, History And Features, Microcontrollers And Embedded Processor, Overview of PIC18 Family.	**Manipulate** the working environment of MPLAB Software
2	Assembly Language Programming, The WREG Register In The PIC, PIC File Registers, PIC Status Register, PIC Data Format And Directives. [1]	**Display** the response of PIC microcontroller by applying different programs. [1]
3	Branch, Call And Time Delay Loop, Branch Instructions And Looping, Call Instructions And Stack, PIC 18 Time Delay	**Construct** different types of circuits on PROTEUS 7.4 professional software.
4	PIC I/O Port Programming, I/O Bit Manipulation Programming. [2]	**Measure** the response of Stepper Motor, Dc Motor & Servo Motor when it interface with PIC Microcontroller. [2]
5	PIC Arithmetic & Logic Instructions And Programs, BCD And ASCII Conversion (Asm and C language). [3]	**Measure** the response of Arithmetic & Logical operation. [3]
6	PIC 18f Hardware Connection, PIC 18f Pin Connection, PIC 18f Configuration Registers, C language programming for PIC interfacing. [4]	**Display** the message on LCD using PIC microcontroller. [4]
7	PIC 18f Timer Programming, Programming Timer 0 And Timer 1, Counter Programming (Asm and C language).	**Manipulate** the working environment of Micro-C pro Software.
8	**Midterm**	
9	PIC 18f Serial Port And ADC Programming, [5]	**Display** the response of PIC microcontroller ADC command set and display on seven segment. [5]
10	FPGA Introduction, FPGA Comparison With PLD And ASICs, Major FPGA Vendors FPGA Families. FPGA Nomenclature and architecture Circuit	**Manipulate** the working environment of Xilinx ISE Project Navigator.

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	Design of FPGA, Logic Elements, Interconnect Logic Design Process, VHDL programing for Digital Design With FPGA. [6]	
11	Conditional concurrent signal assignment for cascaded multiplexers, Flip-Flops, Latches and registers in VHDL.[7]	**Construct** Half adder and Full adder circuit in Xilinx FPGA board using VHDL [6]
12	Selected concurrent signal assignment, Combinational Logic, Arithmetic Logic, Counters. Sequential Machines Counters and Registers. [8]	**Construct** Multiplexer & De-multiplexer circuits in FPGA using VHDL. [7]
13	Finite-State Machine Theory, Design of Mealy Machine using VHDL. [9]	**Construct** the response of FPGA in BCD Counter & Comparator. [8]
14	Design of Moore Machine using VHDL Examples of Complex engineering problem using Mealy and Moore machine	**Construct** the algorithm of vending machine using Finite State Machines in FPGA. [9]
15	Introduction to Arduino and its interfacing	OPEN ENDED LAB
16	Arduino Interfacing, Arduino Introduction And Programming.	Final Viva

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LECTURE PLAN

Course Title: Embedded System Design and Application Course
Code: EE-423

Week No.	Week Dates	Topics	Required Reading	Key Date	CLO-PLO
1	13-03-2022 to 18-03-2022	PIC Microcontrollers, History And Features, Microcontrollers And Embedded Processor, Overview of PIC18 Family.	Pg 1-6 Mazadi		CLO1-PLO1
2	20-03-2022 to 25-03-2022	Assembly Language Programming, The WREG Register In The PIC, PIC File Registers, PIC Status Register, PIC Data Format And Directives.	Pg 17-65 Mazadi		CLO1-PLO1
3	27-03-2022 to 01-04-2022	Branch, Call And Time Delay Loop, Branch Instructions And Looping, Call Instructions And Stack, PIC 18 Time Delay	Pg 75-95 Mazadi	Assignment#1	CLO1-PLO1 CLO2-PLO2
4	04-04-2022 to 08-04-2022	PIC I/O Port Programming, I/O Bit Manipulation Programming.	Pg 107-121 Mazadi		CLO1-PLO1 CLO2-PLO2
5	11-04-2022 to 15-04-2022	PIC Arithmetic & Logic Instructions and programs, BCD and ASCII Conversion (ASM and C language).	Pg 133-162 Mazadi	Quiz # 1	CLO1-PLO1 CLO2-PLO2
6	18-04-2022 to 22-04-2022	PIC 18f Hardware Connection, PIC 18f pin connection, PIC 18f Configuration registers, C language programming for PIC interfacing.	Pg 229-264, 313-332 Mazadi		CLO1-PLO1 CLO2-PLO2
7	25-04-2022 to 29-04-2022	PIC 18f Timer Programming, Programming Timer 0 And Timer 1, Counter Programming (Asm and C language).	Pg 333-340, Mazadi	Assignment #2	CLO2-PLO2 CLO3-PLO3
8	02-05-2022 to 06-05-2022	PIC 18f Serial Port And ADC Programming.	Pg 365-392 Pg 477-499 Mazadi		CLO2-PLO2 CLO3-PLO3
9	**Midterm Examination (10-05-2022 to 14-05-2022)**				
10	16-05-2022 to 20-05-2022	FPGA Introduction, FPGA Comparison with PLD And ASICs, Major FPGA Vendors FPGA Families. FPGA Nomenclature and	Pg 1 – 21 Wayne	Quiz # 2	CLO1-PLO1 CLO2-PLO2

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		architecture Circuit Design of FPGA, Logic Elements, Interconnect Logic Design Process, VHDL programing for digital design with FPGA.			
11	23-05-2022 to 27-05-2022	Conditional concurrent signal assignment for cascaded multiplexers, Flip-Flops, Latches and registers in VHDL.	Pg 165 – 207 Wayne	Assignment#3	CLO2-PLO2 CLO3-PLO3
12	30-05-2022 to 03-06-2022	Selected concurrent signal assignment, Combinational Logic, Arithmetic Logic, Counters, Sequential Machines Counters and Registers.	Pg 228 – 245 Wayne		CLO2-PLO2 CLO3-PLO3
13	06-06-2022 to 10-06-2022	Finite-State Machine Theory, Design of Mealy Machine using VHDL.	Pg 309 – 319 Wayne		CLO2-PLO2 CLO3-PLO3
14	13-06-2022 to 17-06-2022	Design of Moore Machine using VHDL examples of Complex engineering problem using Mealy and Moore machine	Pg 320 – 328 Wayne Pg 329 – 340 Wayne		CLO2-PLO2 CLO3-PLO3
15	20-06-2022 to 24-06-2022	Introduction to Arduino and its interfacing	Pg 7 - 14 Pg 35 – 44 Julien	Quiz # 3	CLO1-PLO1 CLO2-PLO2
16	20-06-2022 to 24-06-2022 (M)	Arduino Interfacing, Arduino Introduction and Programming.	Pg 150 – 170 Pg 254 – 260 Julien		CLO2-PLO2 CLO3-PLO3
Final Examination (28-Jun-2022 to 8-Jul-2022) (14-Jul-2022 to 17-Jul-2022)					

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LAB PLAN

Course Title: Embedded System Design and Application
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Week No.	Lab Date	Objective	Required Reading Lab Manual (Pg-No)
1	13-03-2022 to 18-03-2022	**Manipulate** the working environment of MPLAB Software	2-4
2	20-03-2022 to 25-03-2022	**Display** the response of PIC microcontroller by applying different programs.	5-6
3	27-03-2022 to 01-04-2022	**Construct** different types of circuits on PROTEUS 7.4 professional software.	7-11
4	04-04-2022 to 08-04-2022	**Measure** the response of Stepper Motor, Dc Motor & Servo Motor when it interface with PIC Microcontroller	12-19
5	11-04-2022 to 15-04-2022	**Measure** the response of Arithmetic & Logical operation.	20-21
6	18-04-2022 to 22-04-2022	**Display** the message on LCD using PIC microcontroller	22
7	25-04-2022 to 29-04-2022	OPEN ENDED LAB	23
8	02-05-2022 to 06-05-2022	**Display** the response of PIC microcontroller ADC command set and display on seven segment.	24-25
9	**Midterm Examination (10-05-2022 to 14-05-2022)**		
10	16-05-2022 to 20-05-2022	**Manipulate** the working environment of Xilinx ISE Project Navigator.	26-32
11	23-05-2022 to 27-05-2022	**Construct** Half adder and Full adder circuit in Xilinx FPGA board using VHDL	33-34
12	30-05-2022 to 03-06-2022	**Construct** Multiplexer & De-multiplexer circuits in FPGA using VHDL	35-37

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13	06-06-2022 to 10-06-2022	**Construct** the response of FPGA in BCD Counter & Comparator.	38-39
14	13-06-2022 to 17-06-2022	**Construct** the algorithm of vending machine using Finite State Machines in FPGA.	40-41
15	13-06-2022 to 17-06-2022 (M)	OPEN ENDED LAB	42
16		**Lab Examination** **(20-06-2022 to 24-06-2022)**	